METHODS AND APPARATUS FOR COMPUTER BUS ERROR TERMINATION

ABSTRACT OF THE DISCLOSURE

In a computer system having a bus architecture, a system and process for isolating a device from a bus without interrupting system operation is described, the system including bus interface logic monitoring and reporting activity on the bus, isolation control logic receiving error signals from error detectors, and isolation switches through which devices are interconnected to the bus, the isolation switches allowing for the isolation of the devices from the bus. The isolation control logic determines the devices to be isolated responsive to the reported error and, in turn, transmits an isolation switch control signal to the isolation switch(es) associated with the identified device(s) to isolate those device(s) from the bus. In some embodiments, errors are reported by system software, input/output virtual address error detectors for systems using virtual memory addressing, protocol error detectors, and sensors sensing the physical removal of a bus-connected device from its bus interface slot.